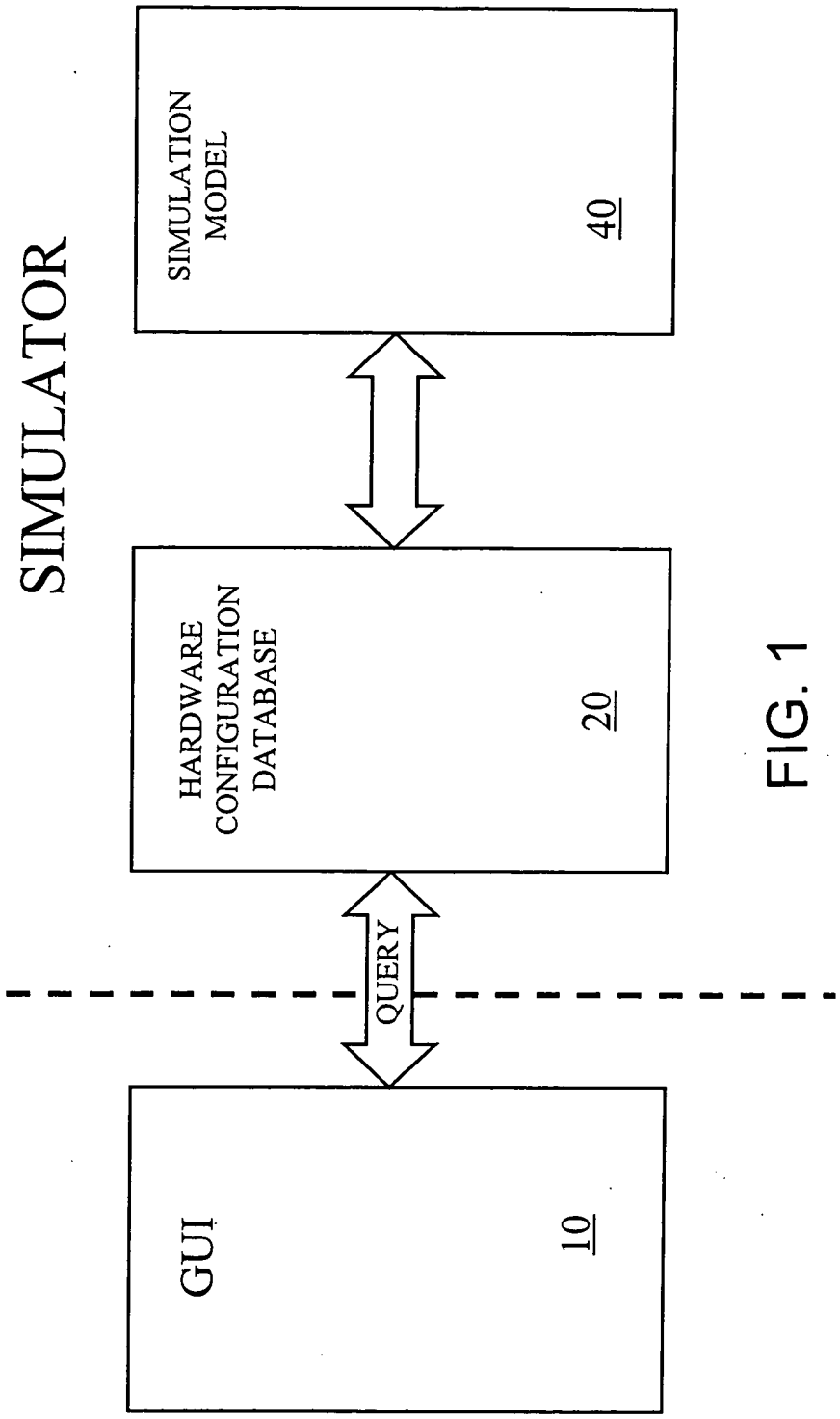
SIMULATOR
SIMULATION MODEL
40
HARDWARE CONFIGURATION DATABASE
20
QUERY
GUI
10

FIG. 1

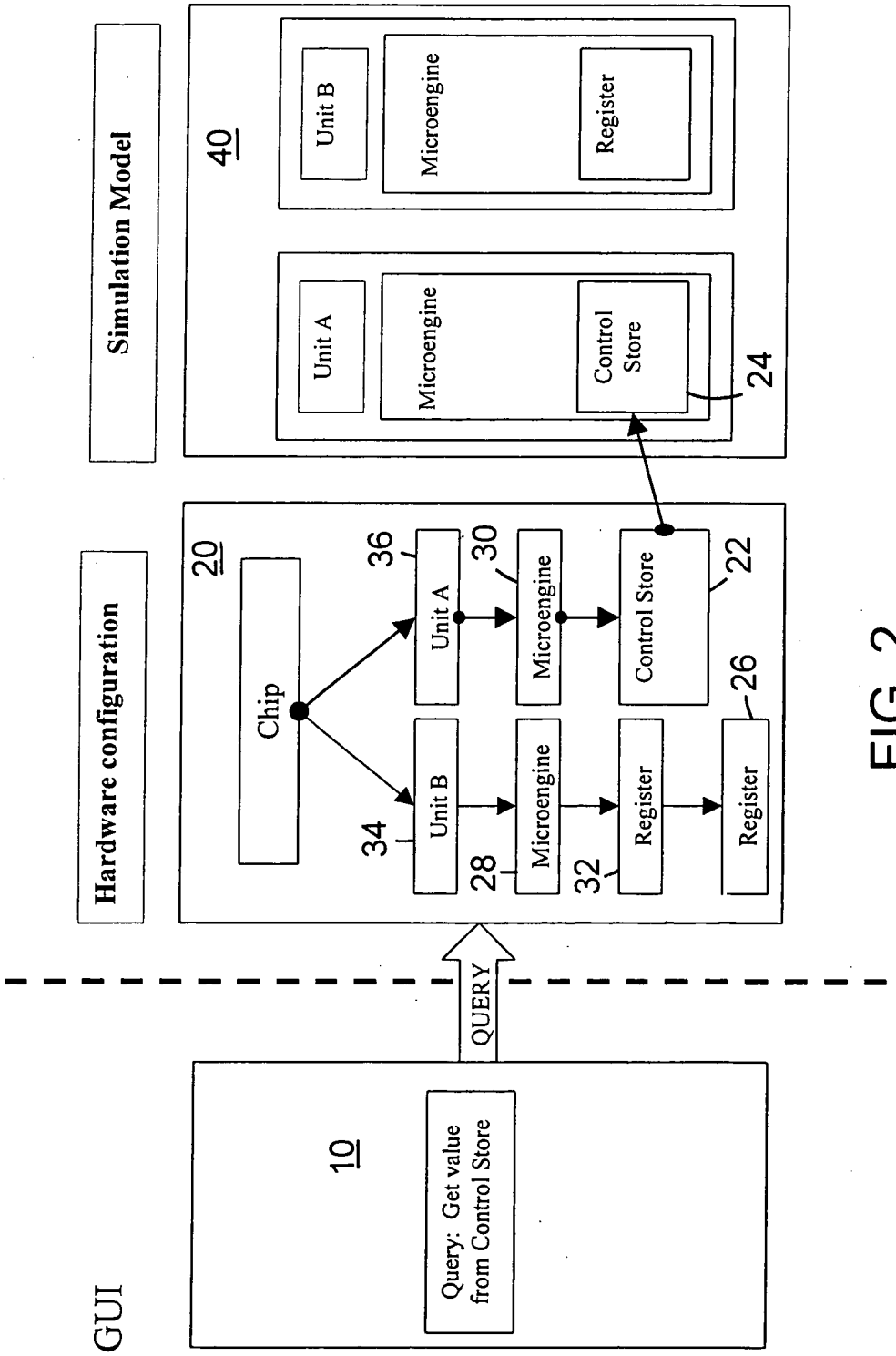
GUI
10
Query: Get value from Control Store
QUERY
Hardware configuration
20
Chip
36
Unit A
30
Microengine
Control Store
22
34
Unit B
28
Microengine
32
Register
Register
26
Simulation Model
40
Unit A
Microengine
Control Store
24
Unit B
Microengine
Register

FIG. 2

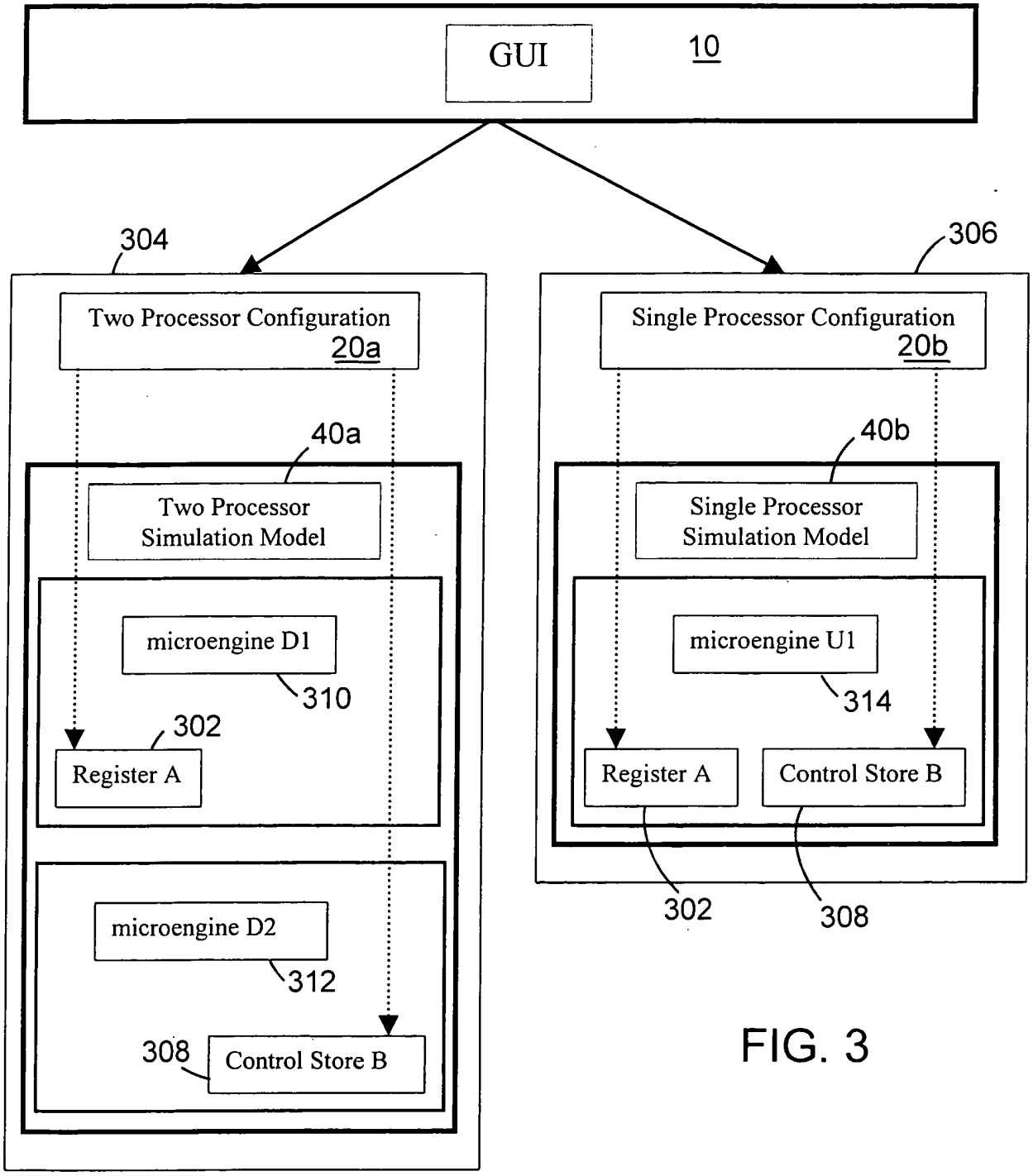
GUI
10
304
306
Two Processor Configuration
20a
Single Processor Configuration
20b
40a
40b
Two Processor Simulation Model
Single Processor Simulation Model
microengine D1
310
microengine U1
314
302
Register A
Register A
Control Store B
microengine D2
312
302
308
308
Control Store B

FIG. 3

```
DEF_CLOCK( K_CORE_CLK, clk );
DEF_USTORE( 312.ram_ustore, ustore );
DEF_ARRAY( 312.TE_GPR_AREG_FILE, gpr_a_regs );
```

FIG. 4A

```
DEF_CLOCK( K_CORE_CLK, clk );
DEF_USTORE( 314.ram_ustore, ustore );
DEF_ARRAY( 314.TE_GPR_AREG_FILE, gpr_a_regs );
```

FIG. 4B

```
S_hw_config_chip *chip = new S_hw_config_chip( m_sim, this );
m_sim->m_hw_config_root->link_chip( chip );

S_hw_config_hw_unit *group = new S_hw_config_hw_unit();
chip->link_subunit( group );

S_hw_config_useq *useq = new S_hw_config_useq_fbox();
group->link_subunit( useq );

useq->associate_ustore( ustore, S_CONFIG_ARRAY__ME_USTORE );
useq->associate_array( gpr_a_regs, S_CONFIG_ARRAY__GPR_A );
```

FIG. 5

```
S_hw_config_chip *chip;
S_hw_config_hw_unit *subunit, *subunit_lower;
S_hw_config_sim *root;
S_hw_config_array *array;
int matches;


root = S_sim::getsim()->m_hw_config_root;
chip = root->m_chip_table[0];
subunit = chip->m_subunit_table[0];


root->find_unique_array( S_CONFIG_ARRAY__ME_USTORE,
&matches );
root->find_unique_array( S_CONFIG_ARRAY__GPR_A,
&matches );
```

FIG. 6